Control System Design

Lecture 9

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Elective Course in Mechatronics Engineering
Credits (2/2/3)

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Motivation: General Remarks

Design Goals

- Good reference tracking (zero steady-state error and fast response, no overshoot)
- Good disturbance rejection
- Attenuation of noise

General Constraints

- Plant dynamics
- Present disturbances
- Sensor dynamics (physical sensor system)
- Actuator dynamics (physical actuator)

Delay Plants: Basic Constraint

Block Diagram

Gap 1

Assumptions

- Disturbance acts after plant delay τ
- C is such that all closed-loop poles lie in the complex left half plane
  $\Rightarrow$ Closed loop is internally stable

Constraint

- Reaction to disturbance d cannot pass the plant before delay τ
  $\Rightarrow$ Not possible to cancel (reject) d in output y before delay τ
  $\Rightarrow$ Best achievable sensitivity: $S(s) = G_2(s)(1 - e^{-s\tau})$

Delay Plants: Limitations

Illustration

Gap 2

Delay Plants: Example

Room Temperature

Gap 3

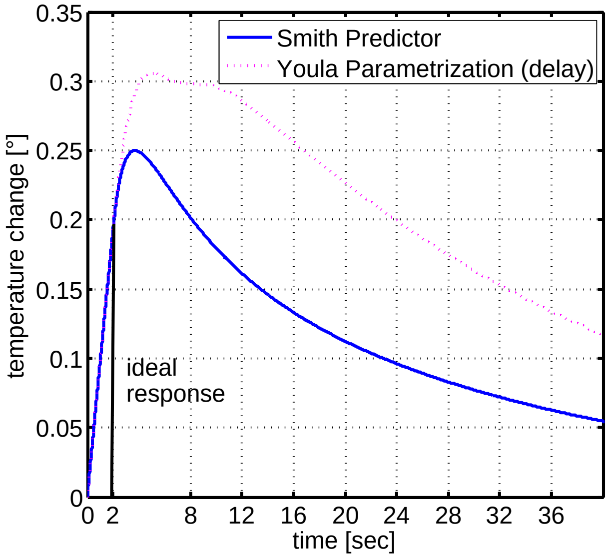
Example Design (Smith-Predictor)

- $G(s) = \dfrac{5e^{-2s}}{1+30s}$
- $C(s) = \dfrac{(1+7s)(1+30s)}{30s^2+s+5(1-e^{-2s})(1+7s)}$

Observation

- Delayed response since $\tau = 2$

Disturbance Step



- Worse than ideal sensitivity due to plant and controller dynamics

Open-loop Integrators: Reference and Output Disturbance

Block Diagram

Gap 4

Characterization

- Plant $G(s) = \dfrac{B(s)}{A(s)}$, controller $C(s) = \dfrac{P(s)}{L(s)}$
- Open-loop denominator $V(s)$ with i integrators

$$V(s) = A(s)L(s) = s^i \cdot V'(s)$$

- General assumption: $B(0) \neq 0$, $V'(0) \neq 0$ and $P(0) \neq 0$

Open-loop Integrators: Examples

Illustration

Gap 5

Open-loop Integrators: Error Step Responses

Error for Output Disturbance or Reference Step

$$\frac{E(s)}{R(s)} = \frac{E(s)}{D(s)} = S(s) = \frac{1}{1 + C(s)G(s)} = \frac{s^i V'(s)}{s^i V'(s) + B(s)P(s)}$$

Steady-state Error

Gap 6

$$\lim_{t \to \infty} e(t) = 0 \text{ for } i > 0$$

Open-loop Integrators: Error Step Responses

Integrated Error

Gap 7

$$\lim_{t\to\infty}\int_0^t e(t)dt = 0 \text{ for } i > 1$$

Implication

1. Reference and output disturbance steps are canceled in the steady state by integrator in the open loop (controller or plant)
2. There is overshoot in y if there is a double integrator in the open loop ($e(t)$ must change its sign)

Open-loop Integrators: Error Step Responses

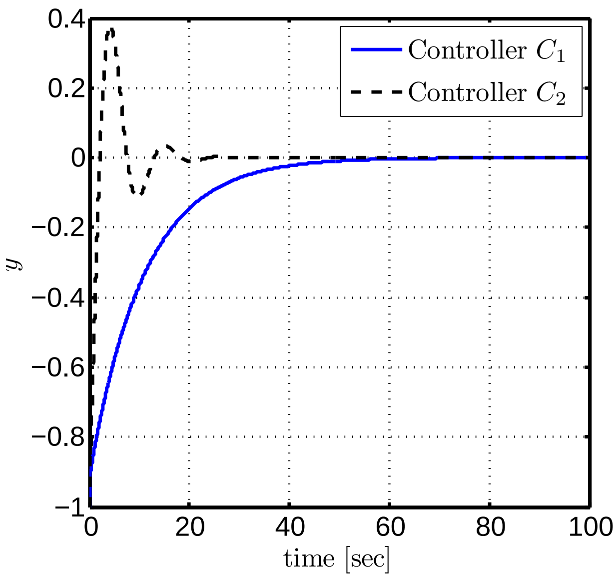
Example Components

- Plant: $G(s) = \dfrac{s+4}{s(s+10)}$
- Controller: $C_1(s) = \dfrac{4+4s}{s+4}$
- Controller: $C_2(s) = \dfrac{1+s}{s}$

Observation

- Zero steady-state error for disturbance rejection in both cases
- Overshoot for double integrator in open loop (C_2)

Output Disturbance Step



Open-loop Integrators: Error Ramp Response

Computation for Output Disturbance or Reference Ramp

$$\frac{E(s)}{R(s)} = \frac{E(s)}{D(s)} = S(s) = \frac{s^i V'(s)}{s^i V'(s) + B(s)P(s)} \text{ for } R(s) = D(s) = \frac{1}{s^2}$$

Steady-state Error

$$\lim_{t\to\infty} e(t) = \begin{cases} 0 & \text{for } i > 1 \\ \frac{V'(0)}{B(0)\,P(0)} & \text{for } i = 1 \end{cases}$$

Integrated Error

$$\lim_{t\to\infty} \int_0^t e(t)dt = 0 \text{ for } i > 2$$

Implication

3. Zero steady-state error for ramps for double integrator in open loop
4. There will be overshoot if there are three integrators in open loop

Open-loop Integrators: Example

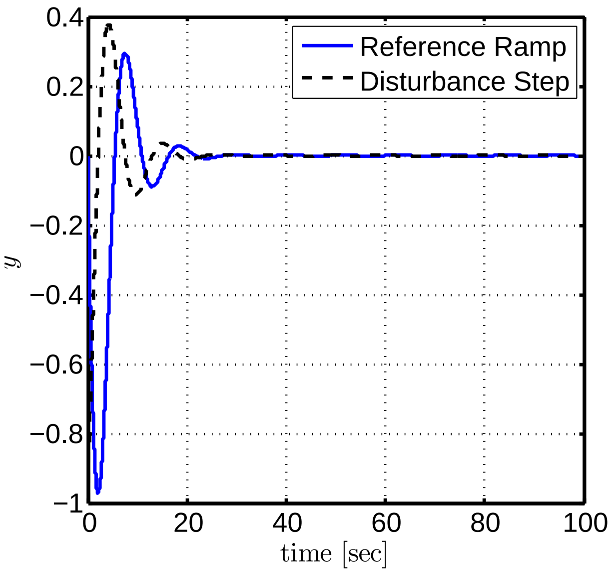
Design Problem

- Plant $G(s) = \frac{1+s}{s}$
- Design a controller with zero steady-state error for ramp reference inputs and that does not produce overshoot for step output disturbances

Gap 8

Open-loop Integrators: Example Simulation

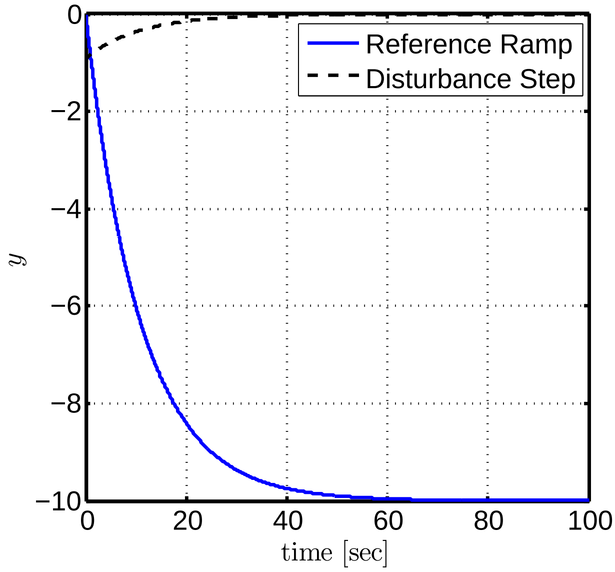
Double Integrator (error signal)



$\Rightarrow G(s) = \frac{s+4}{(s+10)s}$ and $C(s) = \frac{1+4s}{s}$

$\Rightarrow$ Overshoot after disturbance step

Single Integrator (error signal)



$\Rightarrow G(s) = \frac{s+4}{(s+10)s}$ and $C(s) = \frac{1+s}{s+4}$

$\Rightarrow$ Non-zero steady-state error

Integrators and Input Disturbances: Basics

Block Diagram

Gap 9

Sensitivity

$$\frac{Y(s)}{D_i(s)} = S_i(s) = \frac{G(s)}{1 + C(s)\,G(s)} = \frac{B(s)\,L(s)}{A(s)\,L(s) + B(s)\,P(s)}$$

- Consider that $B(0) \neq 0$
  - $\Rightarrow$ Step response: $S_i(0) = 0$ only if $L(0) = 0$
  - $\Rightarrow$ Ramp response: $\lim_{s\to 0} S_i(s)\frac{1}{s} = 0$ only if $\lim_{s\to 0} L(s)\frac{1}{s} = 0$

Integrators and Input Disturbances: Basics

General Result for Input Disturbance Signals $D_i(s) = \frac{1}{s^i}$

- Steady-state error is zero for $L(s) = s^i L'(s)$
  $\Rightarrow$ Controller transfer function needs i integrators
  $\Rightarrow$ Integrators in the plant transfer function (after the entry point of the disturbance signal) are not relevant

Computation

Gap 10

Integrators and Input Disturbances: Example

Computation

Gap 11